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POWER THE FUTURE

AN001

Application Note

HV InnoGaN

Gate Driving Design Guide

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1. Introduction of InnoGaN Gate Driving characteristics

1.1. High-voltage InnoGaN gate characteristics

Driving voltage:

High-voltage InnoGaN integrates ESD protection circuits at the gate terminal to improve gate reliability. The maximum gate-source voltage rating of most InnoGaN products is from -1.4V to +7V. In order to satisfy the negative voltage requirements during off time for high-power applications, the gate negative voltage rating of some products is increased to -6V. The pulsed gate-source voltage range is from -20V to +10V. The drive voltage characteristics of HV InnoGaN are shown as below.

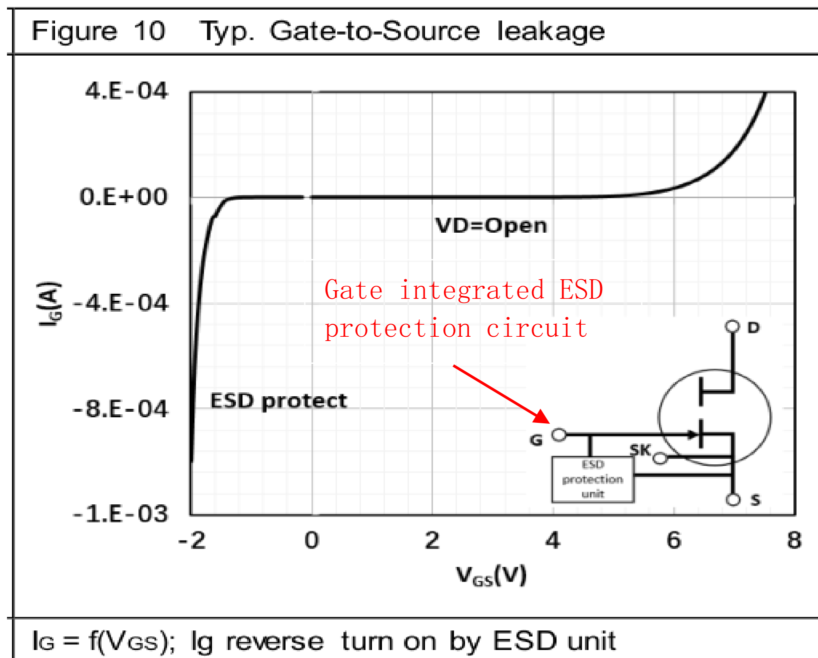


Figure 1 Gate with integrated ESD protection circuit

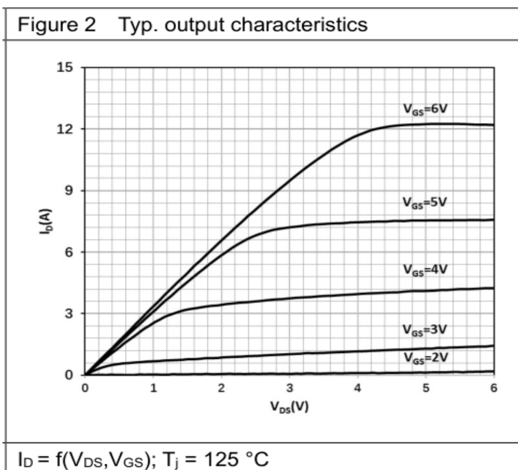
Table 1 Driving voltage characteristics

Symbol	Parameters	Values			Unit	Note/Test-Condition
		Min	Typ	Max		
V_{GS}	Gate source voltage, continuous	-1.4 (-6) ①	-	7	V	T_j = -55 °C to 150 °C
$V_{GSpluse}$	Gate source voltage, pulsed	-20	-	10	V	T_j = -55°C to 150 °C; t_{PULSE} = 50 ns, f = 100 kHz open drain
V_{th}	Gate threshold voltage	1.2	1.6	2.2	V	ID = 11 mA; VDS = V_{GS}; T_j = 25 °C

① For some products, the Gate negative voltage rating is -6V

The relation between gate-source voltage and Rdson:

As shown in Figure 2, for HV InnoGaN, higher gate-source voltage leads to stronger current- capacity and lower the Rdson for the devices. To optimize the performance and reliability of the devices, a high-level gate-source voltage of 6V to 6.5V is recommended.



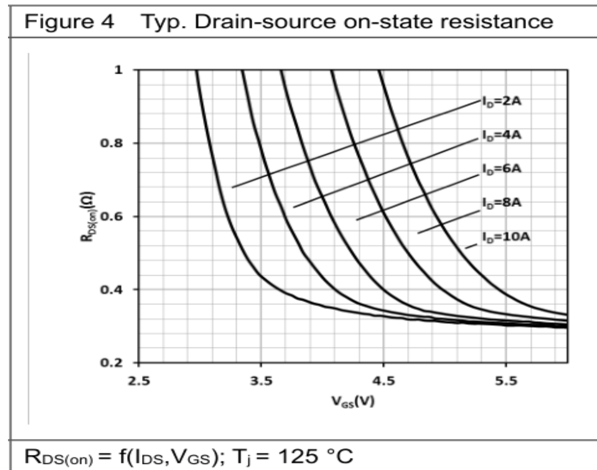


Figure 2 The relation between the Rdson and Vgs of enhancement-mode GaN FETs

1.2. Comparison of HV InnoGaN vs. Si MOSFETs

Similarities:

- High-voltage InnoGaN and enhancement-mode Si MOSFETs are both normally-off power devices.
- Voltage-driven: During the switching process, the drive voltage charges and discharges the parasitic capacitance Ciss/Crss of the device, and provides gate leakage current Igss with positive bias .
- Switching speed could be modified by external gate resistance Rg_ext.

Differences:

- Gate voltage rating and Vth threshold are lower, requiring careful handling of the drive circuit to avoid oscillations leading to fault turn-on/off.
- The recommended drive voltage for HV InnoGaN is 6V, which is lower than the 8~12V for Si MOSFETs. To be compatible with controllers that are designed for Si MOSFETs, voltage divider or additional gate driver are necessary to adapt the gate voltage requirements of HV InnoGaN.

2. Categories of HV InnoGaN gate driving circuits

Table 2 Categories of HV InnoGaN gate driving circuits

Classification			Diagram	Characteristics	Application
Single	Non-isolated	Voltage divider		Compatible with controllers with voltage higher than 6.5V, adjustable drive voltage, adjustable negative voltage turn-off, high anti-interference capability.	**Applications:** fast charger, adapters, LED, TV, electrical tools, etc. **Topology:** Flyback、PFC、Forward
				Compatible with controllers with voltage higher than 6.5V, adjustable drive voltage, adjustable negative voltage turn-off, high anti-interference capability.	**Applications:** fast charger, adapters, LED, TV, electrical tools, etc. **Topology:** Flyback、PFC、Forward
		Direct-driving		Direct drive with 6V Vcc, simple circuit, small gate driving loop, low interference.	**Applications:** fast charger, adapters, LED, TV, electrical tools, etc. **Topology:** Flyback、PFC、Forward
Half-Bridge	Non-isolated	Voltage divider		Compatible with controllers for Si MOSFETs , adjustable drive voltage, capable of negative voltage during off time.	**Applications:** medium to low-power supplies, such as LED, adapters, etc. **Topology:** AHB, LLC, ACF.

		Direct-driving		Simple gate driving circuit, capable of direct drive for GaN.	**Applications:** medium to low-power supplies, such as LED, adapters, etc. **Topology:** AHB, LLC, ACF.
	Isolated	Digital isolator + Driver		High reliability , negative voltage during off time, discrete driver could be placed close to GaN for optimized gate driving loop design.	**Applications:** high-power supplies, such as communication and server power supplies. **Topology:** Totem-pole PFC, LLC.
		Integrated digital isolator + Driver		High reliability, negative voltage during off time, integrated isolated half-bridge driver for simplified drive design.	**Applications:** high-power supplies, such as communication and server power supplies. **Topology:** Totem-pole PFC, LLC.

3. Single GaN Gate Driving Design

3.1. Voltage Divider Gate Driving

3.1.1. Circuit Diagrams

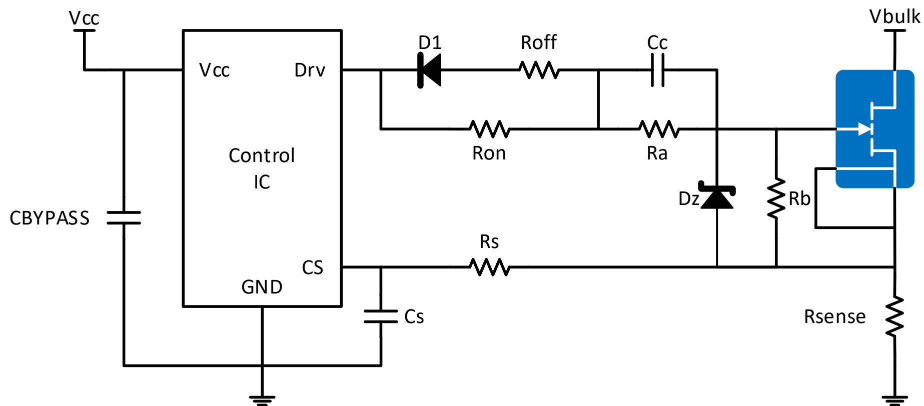


Figure 3 Voltage divider driver circuit(Suitable for gate voltage range of -1.4V to +7V)

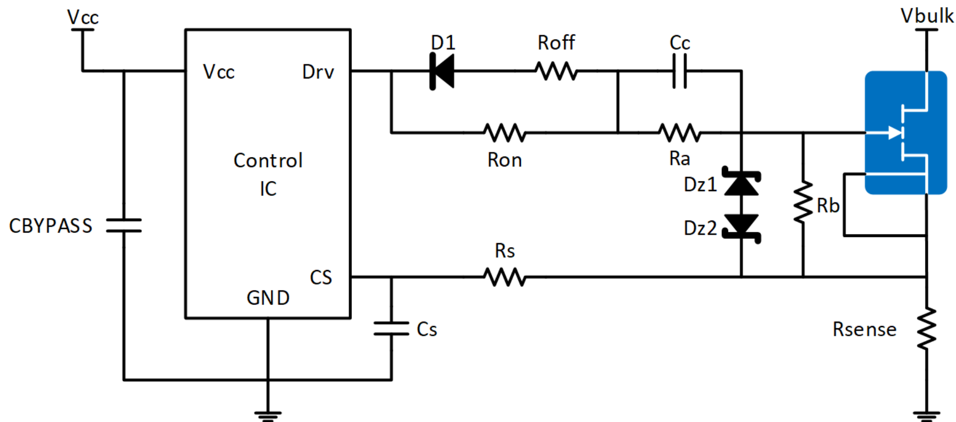


Figure 4 Voltage divider driver circuit(Suitable for gate voltage range of -6V to +7V)

3.1.2. Functions of Components in Voltage Divider Gate Driving Circuits

Table 3 Functions of Components in Voltage Divider Gate Driving Circuits

Component	Functions
Ron	Modify the turn-on speed GaN FET
Roff	Modify the turn-off speed GaN FET
Dz/Dz1	Clamping the gate voltage of GaN FET
Ra	Voltage dividing resistor
Rb	
CC	Switching acceleration capacitor
Dz2	Clamp-of negative voltage during off-time

3.1.3. Switching Process with Voltage Divider Gate Driving Circuit

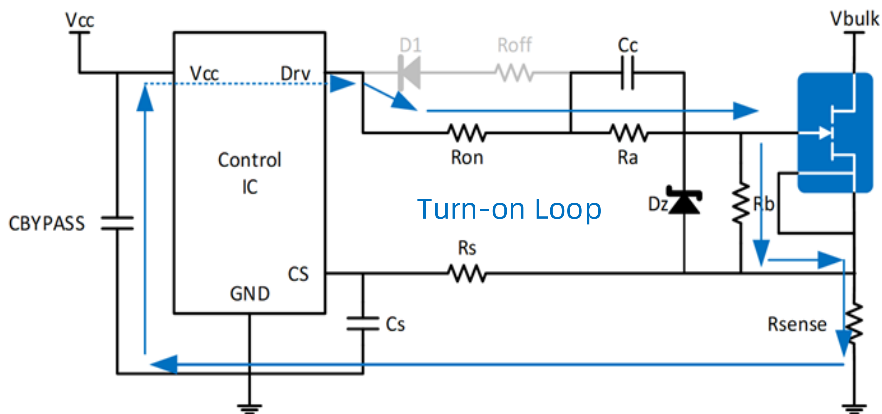


Figure 5 Voltage divider drive turn-on circuit

During the turn-on process, the gate driving current flow is shown in Figure 5, consists of Ron, Ra, Cc, Rb, GaN FET, Rsense, and CBYPASS. VDrv charges the Ciss/Crss of HV InnoGaN quickly through Ron and Cc, making the Vgs voltage to rise rapidly, thus turning on the GaN FET.

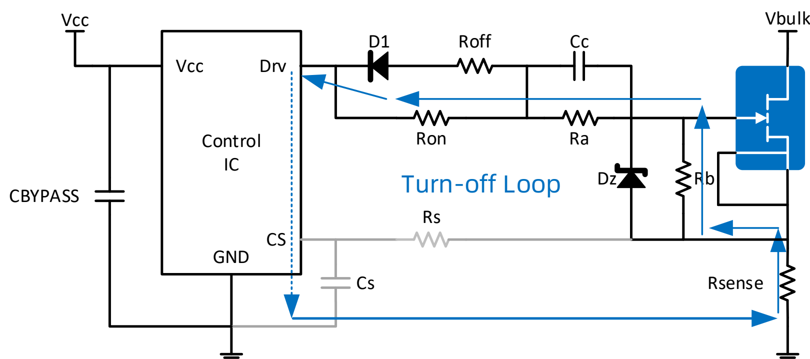


Figure 6 Voltage divider drive turn-off circuit

During the turn-off process, the gate driving current flow is shown in Figure 6, consists of Ron, Roff, D1, Ra, Cc, Rb, Dz, GaN FET, and Rsense. VDrv discharges the Ciss/Crss of high-voltage InnoGaN rapidly through D1, Roff, and Cc, causing the Vgs voltage to decrease quickly, thus turning off the power transistor. After the discharge of Ciss, further discharge of Cc is needed, during which current flows through Dz, generating a negative Vgs voltage.

3.1.4. Voltage Divider Design Consideration

3.1.4.1. Impact of Sensing Resistor on the Gate Voltage

During turn-on process, there will be a certain voltage drop across the sense resistor in the power loop , which affects the Vgs voltage. This voltage drop needs to be considered during parameter design.

3.1.4.2. Impact of Igss on Gate Voltage

During the on time of GaN FET, the driver needs the control IC to provide a current flowing through the zener diode, Rb, and gate terminal of GaN (Igss).,The maximum value of Igss at high temperature should be chosen when design for Igss of GaN increases with temperature.

3.1.4.3. Impact of Cc on Gate Voltage

The resistance of the voltage divider is relatively high, resulting in very low driving current during the switching process and low speed switching of GaN FETs. With the low AC impedance of the capacitor Cc, which is connected in parallel with Ra., most of the current flows through Cc to charge and discharge the Ciss/Crss of GaN FETs during the switching processes and thus achieve fast switching. During the switching processes, Cc and Ciss/Crss are in series, and the charge of Cc must be greater than Ciss/Crss to ensure rapid charging and discharging of Ciss/Crss to effectively turn-on and turn-off the HV InnoGaNs, satisfying the following equation:

$$Cc > Q_{gplat}/V_{plat} \quad (Q_{gpla}t=QGS+QGS)$$

Different capacitance of Cc leads to different driving waveforms. Too small Cc is slows down the switching process , with the risk that GaN FETs could not be turn-on or turn-off in a short time. Given that Cc meets the requirements, a larger Cc results in a longer negative gate-source voltage duration during off time.

The simulated waveforms are shown in in Figure 7. When Cc = 100pF, the turn-on speed is slow, and there is a trailing phenomenon after turn-off action of the device When Cc = 560pF, the turn-on speed is much faster , and

there is an acceptable negative voltage between gate and source after turn-off action of the device. When Cc = 3.3nF, there is a negative gate-source voltage throughout the off time, and the peak negative voltage is clamped as the forward conduction voltage of the Zener diode Dz, ensuring the negative pressure is within -1.4V. The voltage rating of ZD1 and ZD2 are selected as 5.6V.

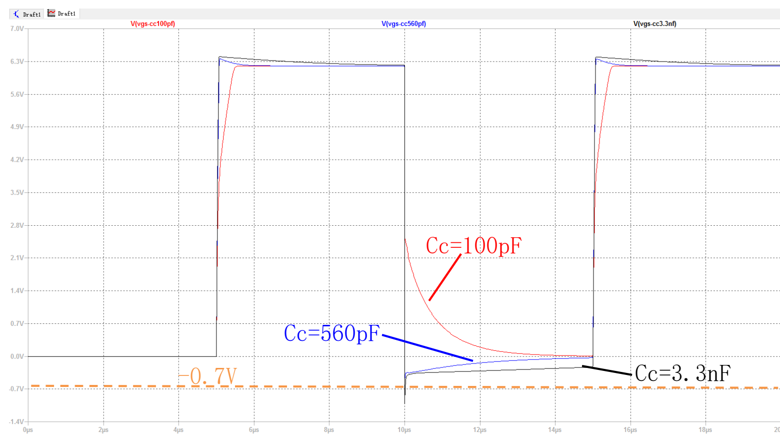


Figure 7 Impact of Cc capacitor on driver(Single Zener circuir)

The influence of Cc on the driving voltage is shown in Figure 8.

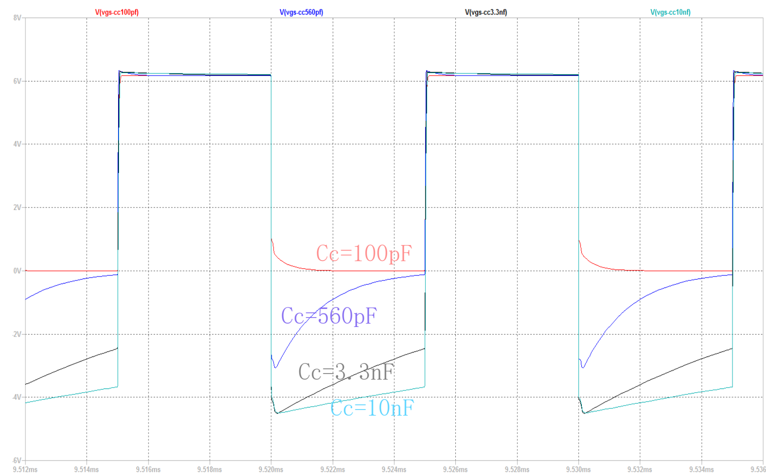


Figure 8 The influence of Cc capacitance on the driving voltage (double Zener circuit)

3.1.4.4. Selection of Zener Diodes

The voltage accuracy, forward voltage drop, and temperature drift should be considered when choosing the Zener diodes. The voltage accuracy of ±2% is recommended. . A 6.2V zener voltage is recommended for ZD, while 5.1V zener voltage is recommended for ZD1 and ZD2.

Table 4 Zener diode and parameters

Device*	Device Marking	Test Current Izt mA	Zener Voltage VZ		Z_{ZK} I_Z = 1.0 mA Ω Max	Z_{ZT} I_Z = IZT @ 10% Mod Ω Max	Max IR @ VR		d_{VZ}/dt (mV/k) @ I_{ZT1} = 5 mA		C pF Max @ V_R = 0 f = 1 MHz
			Min	Max			µA	V	Min	Max	
MM5Z2V4ST1G/T5G	T2	5.0	2.43	2.63	1000	100	120	1.0	−3.5	0	450
MM5Z2V7ST1G	T3	5.0	2.67	2.91	1000	100	100	1.0	−3.5	0	450
MM5Z3V3ST1G	T5	5.0	3.32	3.53	1000	95	5.0	1.0	−3.5	0	450
MM5Z3V6ST1G	T6	5.0	3.60	3.85	1000	90	5.0	1.0	−3.5	0	450
MM5Z3V9ST1G	T7	5.0	3.89	4.16	1000	90	3.0	1.0	−3.5	−2.5	450
MM5Z4V3ST1G	T8	5.0	4.17	4.43	1000	90	3.0	1.0	−3.5	0	450
MM5Z4V7ST1G/T5G	T9	5.0	4.55	4.75	800	80	3.0	2.0	−3.5	0.2	260
MM5Z5V1ST1G/T5G	TA	5.0	4.98	5.2	500	60	2.0	2.0	−2.7	1.2	225
MM5Z5V6ST1G/T5G	TC	5.0	5.49	5.73	200	40	1.0	2.0	−2.0	2.5	200
MM5Z6V2ST1G/T5G	TE	5.0	6.06	6.33	100	10	3.0	4.0	0.4	3.7	185
MM5Z6V8ST1G/T5G	TF	5.0	6.65	6.93	160	15	2.0	4.0	1.2	4.5	155

3.1.5. Examples of voltage divider gate driving design

Example 1:

Driving Parameter Calculation procedure

(Using Controller NCP1342 and HV InnoGaN INN650DA240A as Examples)

1、 Confirm the Known Parameters:

- Minimum Driving Voltage of the Controller: The minimum driving voltage can be found in the datasheet of the controller. VDrv_min = 10V in this case.

Table 5 Driving voltage of NCP1342

Symbol	Parameters	Values			Unit	Note/Test-Condition
		Min	Typ	Max		
$I_{DRV(SRC)}$ $I_{DRV(SNK)}$	Current Capability Source Sink	- -	500 800	- -	mA	
$V_{DRV(high1)}$ $V_{DRV(high2)}$	High State Voltage	8.0 10	- 12	- 14	V	$V_{CC}=V_{CC(off)}+0.2V$, $R_{DRV}=10k\Omega$ $V_{CC}=30V$, $R_{DRV}=10k\Omega$
$V_{DRV(low)}$	Low Stage Voltage	-	-	0.25	V	$V_{Fault}=0V$

- HV InnoGaN Pull-Down Resistance: R_b=10kΩ (recommended in the range of 10-20kΩ)
- Voltage on the current sensing resistor: V_{Rsense}
- Zener Diode : Dz chosen as a 6.2V zener diode with an accuracy of ±2%
- HV InnoGaN gate leakage current: I_{gss_max}=788uA@Tj=125℃
- HV InnoGaN high-level gate voltage : set V_{gs}=6V

2、 Calculation of Voltage Dividing Resistors:

$$Ron + Ra = \frac{VDrv_{min} - Vgs - VRsense}{\frac{Vgs}{Rb} + Igss_max} = 2.132K\Omega$$

3、 Ron is used to regulate the switch speed and optimize EMI performance. The value of Rb depends on the value of Ron.

4、 Calculation of Capacitor Cc :

$Cc > \frac{0.9nC}{2.5V} = 360pF$ (Typically, a value 2-4 times greater than the calculated value is chosen empirically)

Table 6 Gate charge characteristics of INN650DA240A

Symbol	Parameters	Values			Unit	Note/Test-Condition
		Min	Typ	Max		
Q_G	Gate charge		2		nC	V_{GS} = 0 to 6V; V_{DS} = 400V; I_D = 3A
Q_{GS}	Gate-source charge		0.2		nC	
Q_{GD}	Gate-drain charge		0.7		nC	
V_{Plat}	Gate Plateau Voltage		2.5		V	V_{DS} = 400V; I_D = 3A

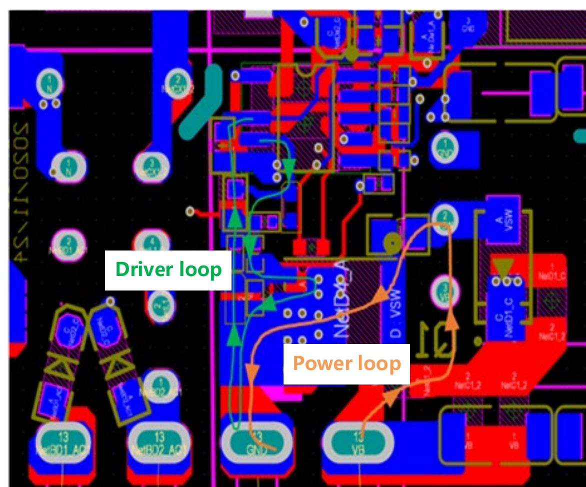


Figure 9 layout reference design

Layout Design Suggestions:

➢ Place the drive pin of the control IC as close as possible to the GaN device to minimize the gate driving loop.

- In a multi-layer PCB design, the drive circuit should be routed parallel on top and adjacent inner layers to minimize the parasitic inductance.
- Avoid the overlap between the driving loop and power loop to minimize the interference between them.
- Maximize the copper area that connected to the thermal pad of InnoGaN to improve thermal performance.

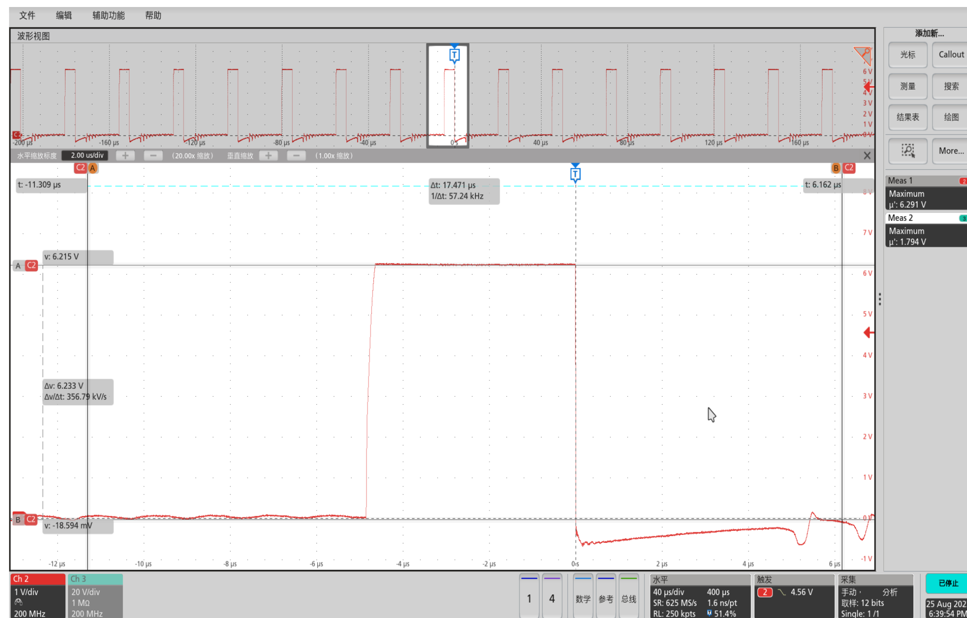


Figure 10 Voltage-divider drive waveform

Example 2: Driving Circuit Design Negative Gate Voltage

By increasing the capacitance, Cc discharges throughout the off time. The discharging current of Cc flows through Rb (10K resistor), and generates a significant voltage drop, providing a high negative voltage to the gate terminal.

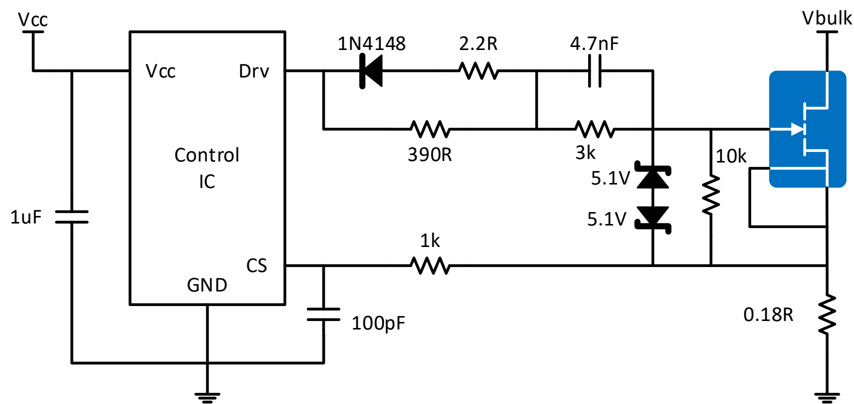


Figure 11 The example of driving design with higher negative voltage

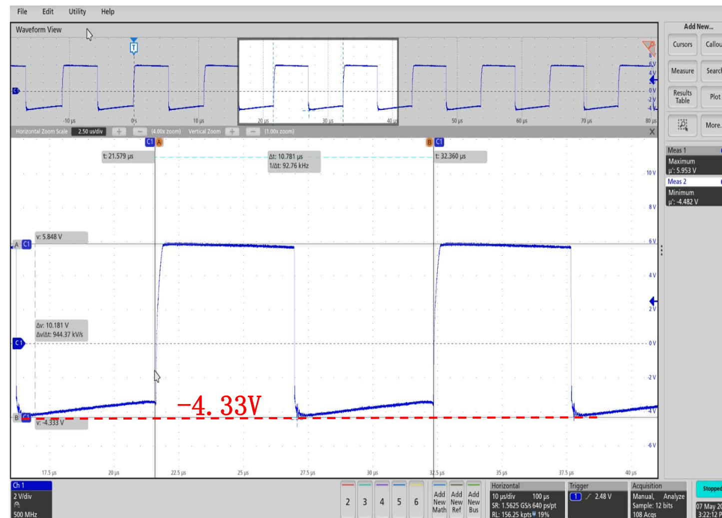


Figure 12 Voltage-Divider Drive Waveform (Large Negative Voltage)

3.2. Direct-driving

3.2.1. Direct-driving circuit

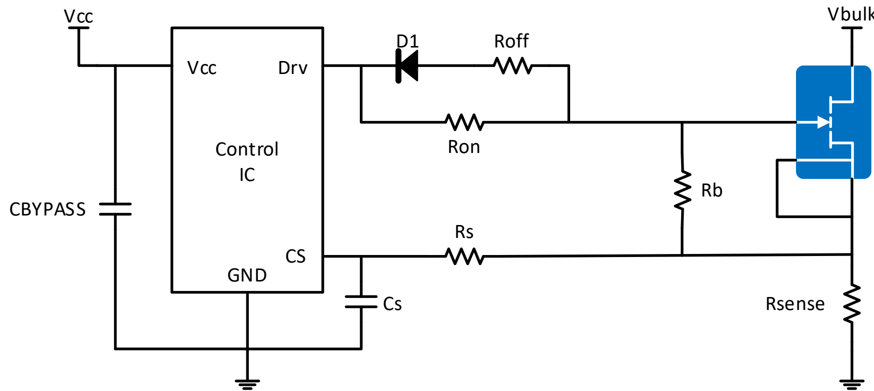


Figure 13 Direct-driving circuit

3.2.2. The functions of each components

Table 7 The functions of each components

Component	Functions
Ron	Modify the turn-on speed of GaN FET
Roff	Modify the turn-off speed of GaN FET
Rb	Gate pull-down resistor

3.2.3. Considerations for Direct-Driving

- Driving ICs with driving voltage of 6V is recommended for the driving voltage varies among different ICs.
- During conduction time, the voltage drop on the sense resistor can cause a slightly voltage drop on the Vgs voltage of GaN. It is recommended to select a control IC with driving voltage compensation or negative current detection.
- Attention should be paid to the impact of Igss on the driving voltage. The recommended driving resistance Ron is within 330Ω.

3.2.4. Example design of direct-driving circuit

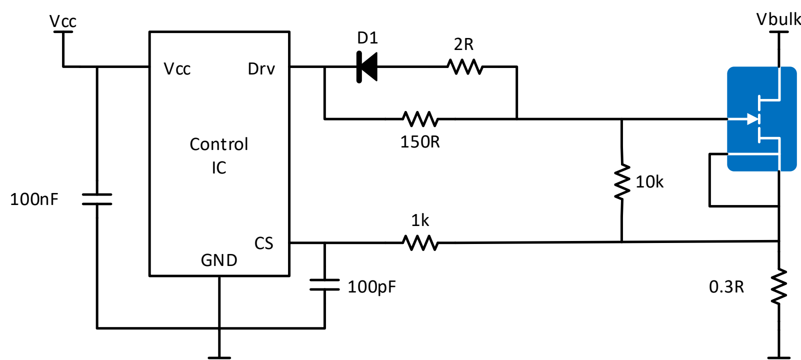


Figure 14 Example of direct-driving circuit

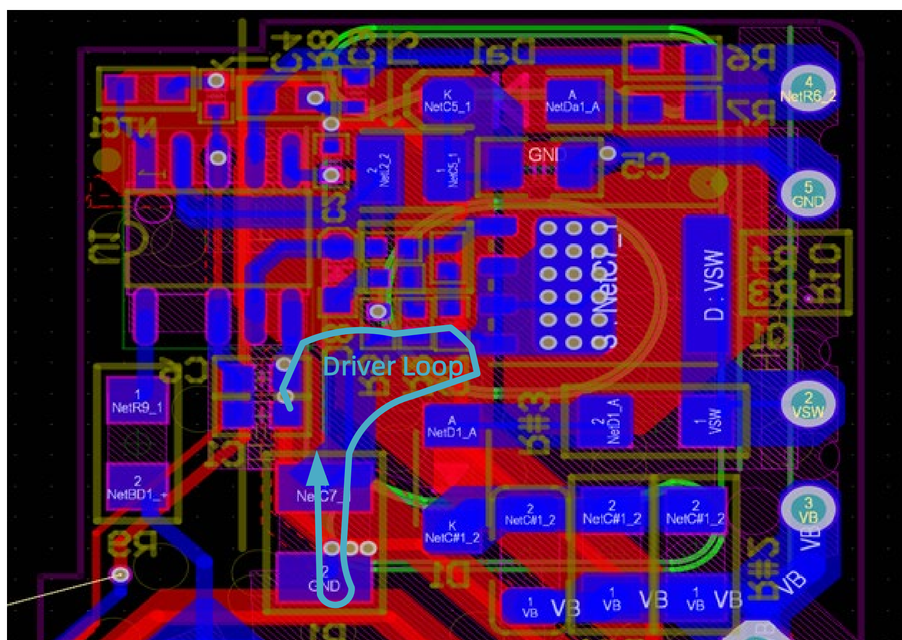


Figure 15 Layout design

- Place the Drive pin of the control IC close to the GaN device, and keep the driving loop as short as possible.
- For multi-layer PCBs, the driving traces can be routed on the top and bottom layers in parallel to reduce parasitic inductance.
- Ensure that the driving circuit and power circuit do not overlap to avoid interference of the power circuit on the driving signals.
- Maximize the copper area for the GaN source heat dissipation pad, and provide additional heat dissipation support.

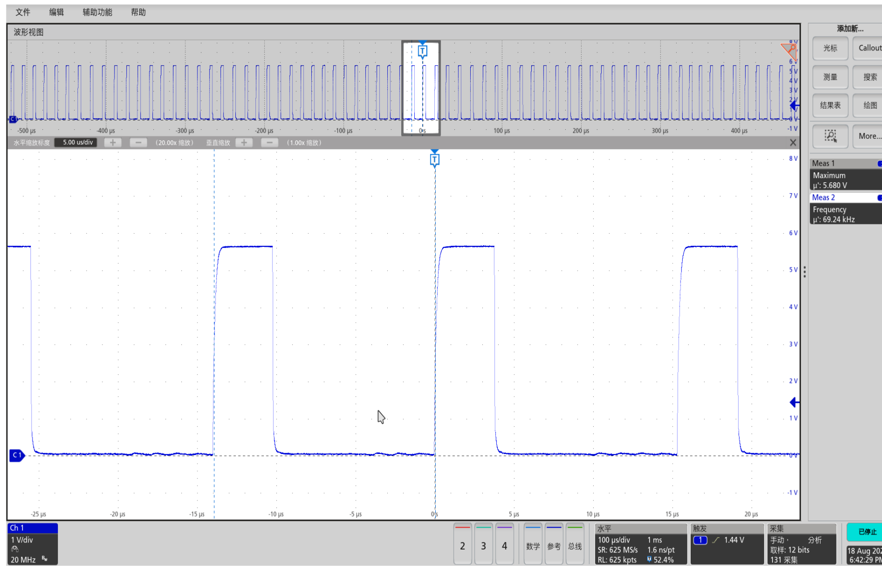


Figure 16 Waveform of direct-driving circuit

4. Half-bridge gate driving design

4.1. Half-bridge non-isolated driving

4.1.1. Half-bridge non-isolated driving circuit

Non-isolated half-bridge driving is suitable for small to medium power applications such as ACF, AHB, LLC, etc. The reliability of the half-bridge driving can be improved with a negative voltage, avoiding short-through between the two devices.

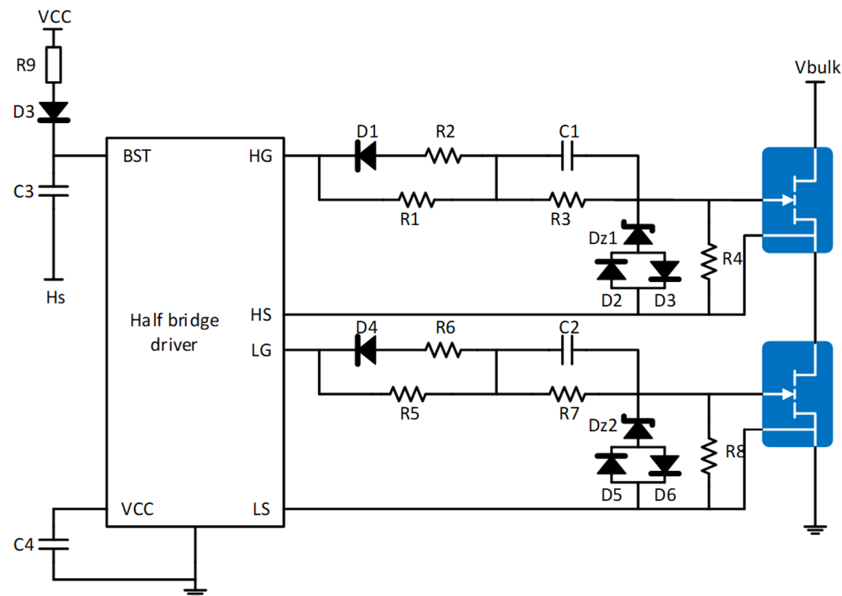


Figure 17 Non-isolated half-bridge driving circuit with voltage divider

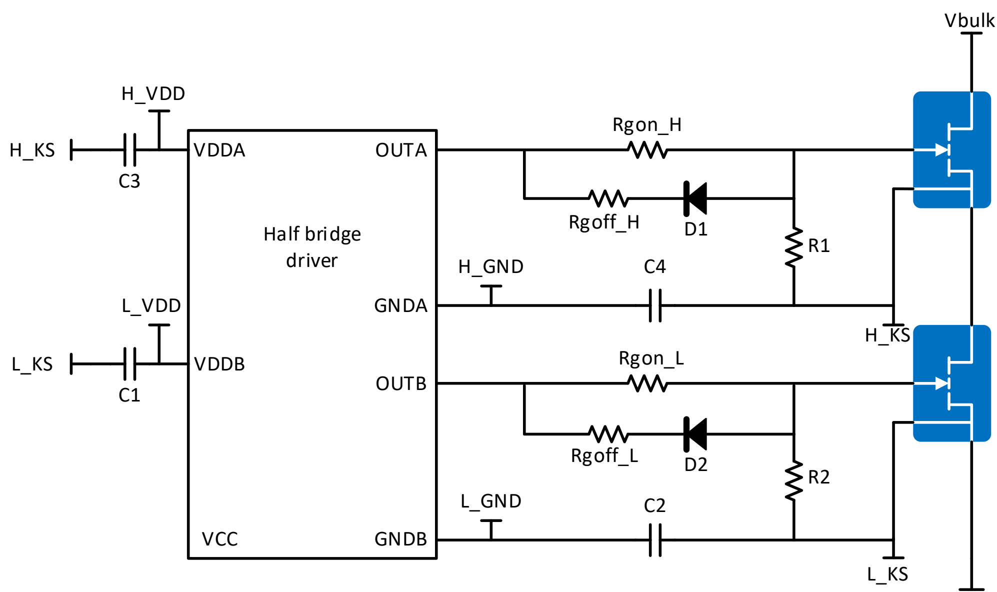


Figure 18 Non-isolated half-bridge direct-driving circuit

4.1.2. The functions of components

Table 8 The functions of Components in a voltage divider circuit

Component	Functions
R1/R5	Adjust turn-on speed of GaN FET
R2/R6	Adjust turn-off speed of GaN FET FET
Dz1/D3/Dz2/D6	Clamping the gate voltage of GaN FET
R3/R7	Voltage divider resistor
R4/R8	
C1/C2	Switching acceleration capacitor
D2/D5	Increase the turn-off negative voltage

Table 9 The functions of Components in a direct-driving circuit

元件	功能
R_{gon_H}/R_{gon_L}	Adjust turn-on speed of GaN FET
R_{goff_H}/R_{goff_L}	Adjust turn-off speed of GaN FET FET
R1/R2	Gate pull-down resistor

4.1.3. Switching process of Half-bridge non-isolated driving

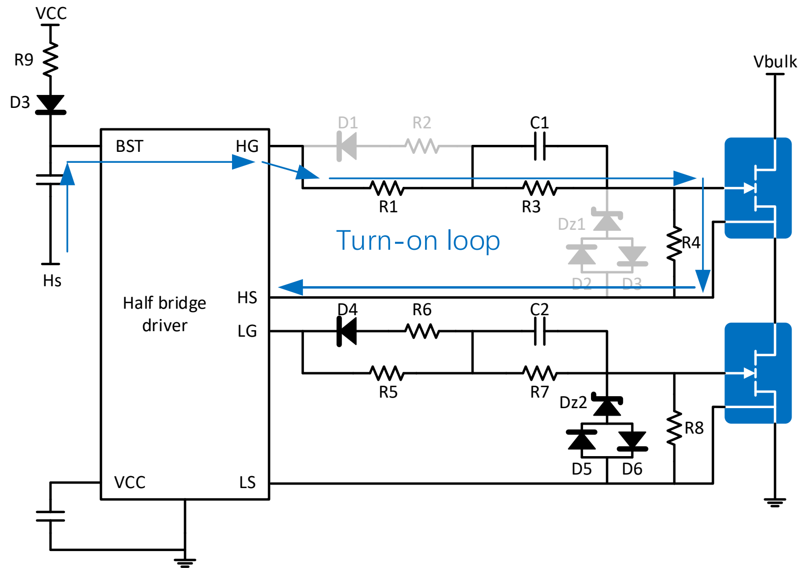


Figure 19 Turn-on loop of Voltage divider circuit

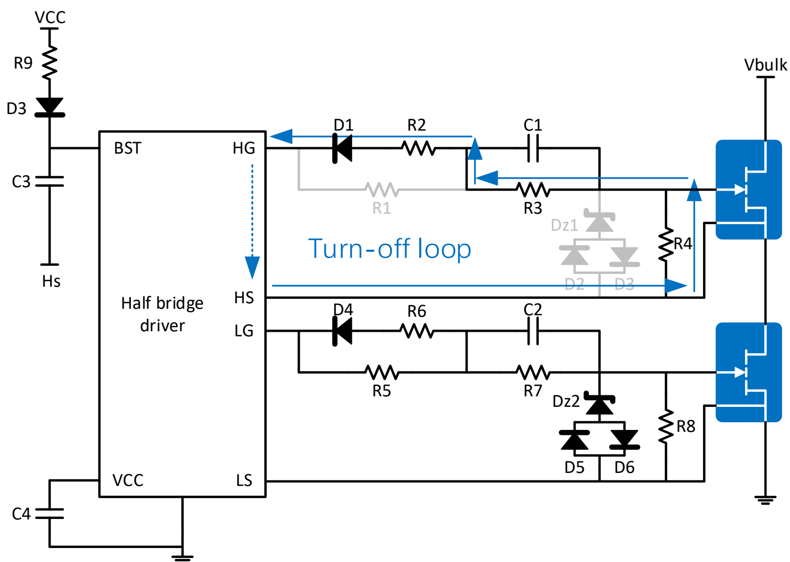


Figure 20 Turn-off loop of Voltage divider circuit

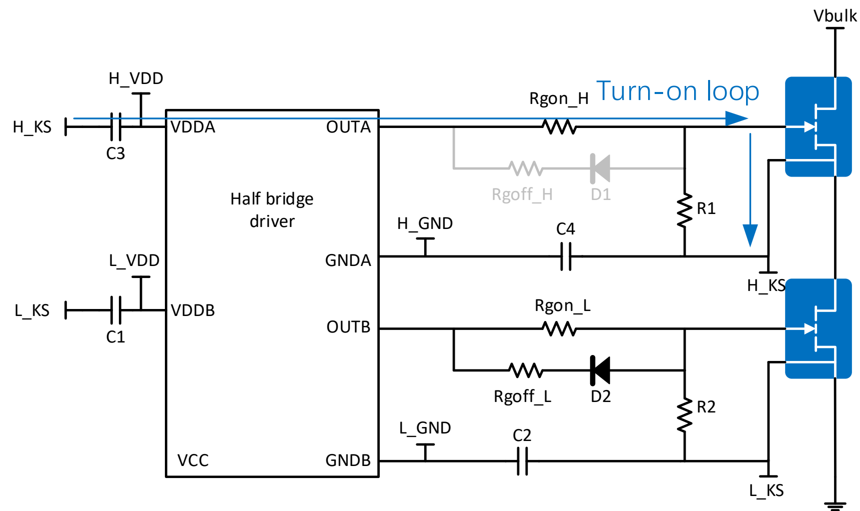


Figure 21 Turn-on loop Direct-driving circuit

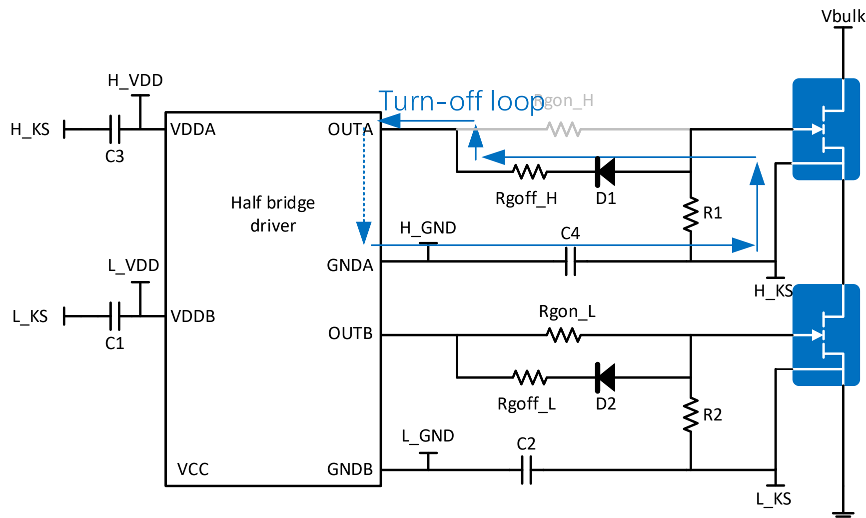


Figure 22 Direct-driving circuit turn-off loop

4.1.4. design example of Half-bridge non-isolated driving circuit

Table 10 Parameters of half-bridge driving circuit with voltage divider

Component	Function	Typical	Range
R1/R5	Modify turn-on speed of GaN FET	390R	360R ~ 510R
R2/R6	Modify turn-off speed of GaN FET	1R	0 ~ 10R
Dz1/Dz2	Clamping the gate voltage of GaN FET	5.6V	5.6V ~ 6.2V
D3/D6		RB521	1N4148(low frequency) Schottky diode(high frequency)
R3/R7	Divider resistor	7.5K	2K ~ 7.5K
R4/R8		10K	2K ~ 10K
C1/C2	Switching acceleration capacitor	2.2nF	2.2nF ~ 3.3nF
D2/D5	Increase the gate-source negative voltage	RB521	1N4148(low frequency) Schottky diode(high frequency)

The negative voltage generating circuit of non-isolated half-bridge direct-driving circuit is shown in Figure 23. The high-level gate-source voltage of high/low-side GaN is determined by the 6.2V zener diodes DZ1/DZ2. The turn-off negative voltage is recommended as -3V which equals to H_VDD/L_VDD - 6.2V,.

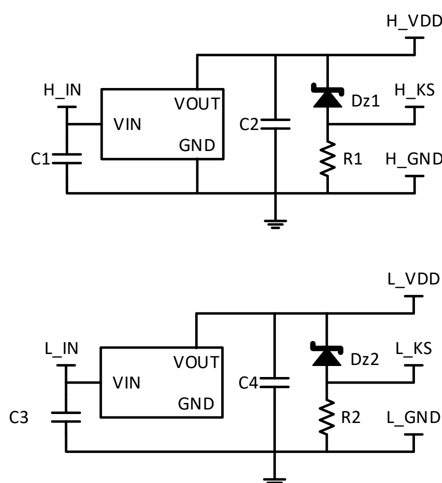


Figure 23 Negative voltage generating circuit for half-bridge direct-driving

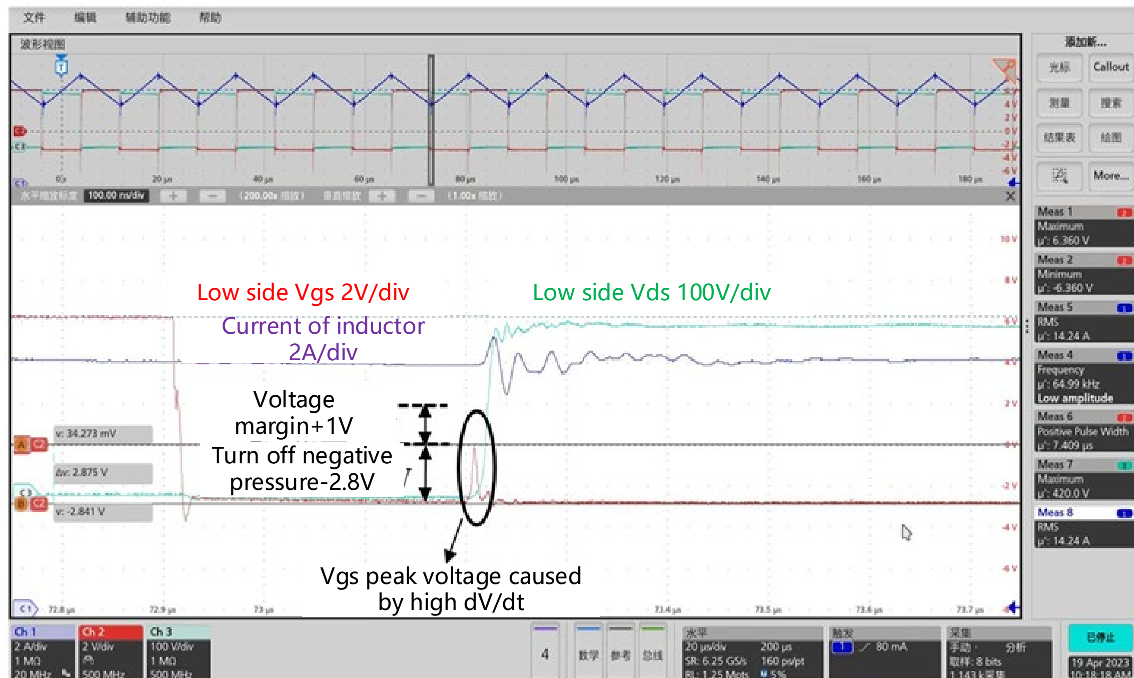


Figure 24 Measured waveforms

4.1.5. Design considerations of Half-Bridge Non-Isolated Driving Circuit

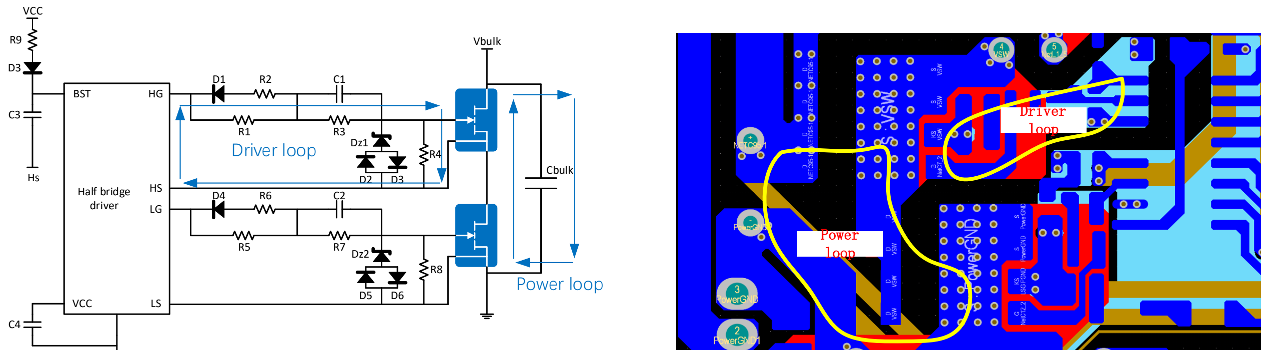


Figure 25 Example of layout design

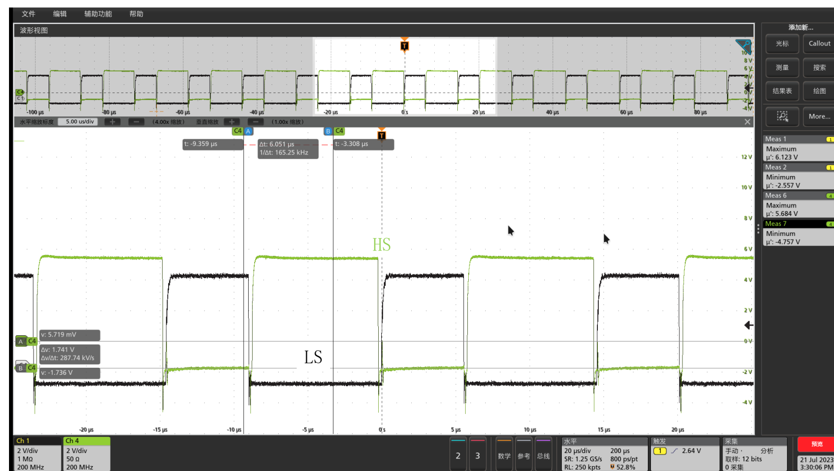


Figure 26 Measured waveforms

- Use Kelvin source design to minimize the coupling between the driving loop and the power loop.
- Place the driver IC as close as possible to the GaN to minimize the loop parasitic inductance.
- Make sure the turn-on path of the driver as small as possible: VCC-DRV-Ron-Cc-Dz//Rb-Cbypass.
- Increase the area of the gate return path to minimize the impedance of the driving loop.
- Keep the driving traces of high-side GaN away from the ground signal side to avoid uncontrollable circulating current.
- Keep noisy traces away from the driving loop to avoid noise coupling.

4.2. Half-bridge isolated driving circuit design

4.2.1. Half-bridge isolated driving circuit

The half-bridge isolated driving circuit is suitable for high-power applications such as totem-pole PFC, LLC topology, with, ensuring high reliability with negative off voltage . Discrete driver ICs could be placed close to GaN FETs , thus benefitting for the driving circuit design. Also, the driving design could be simplified with integrated isolated half-bridge driver .

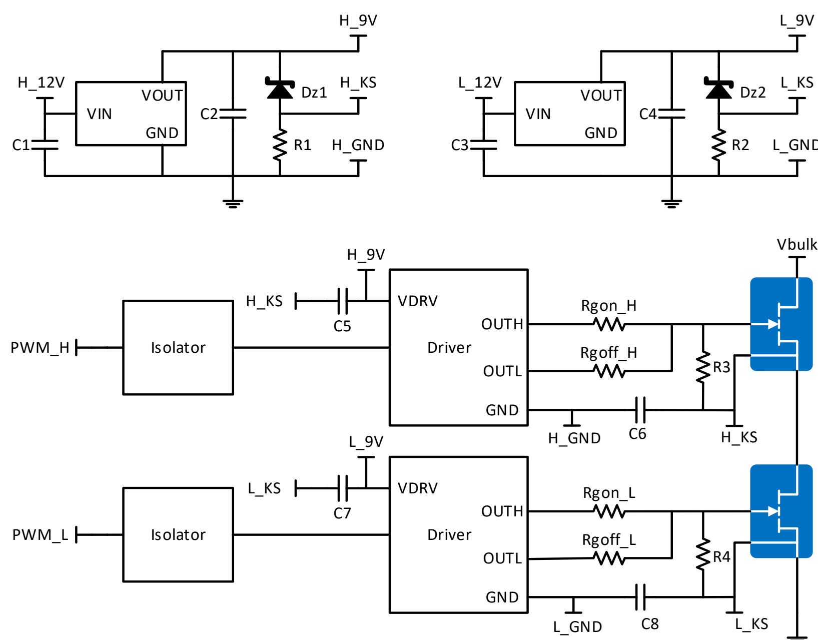


Figure 27 Half-bridge driver circuit with digital isolator + driver

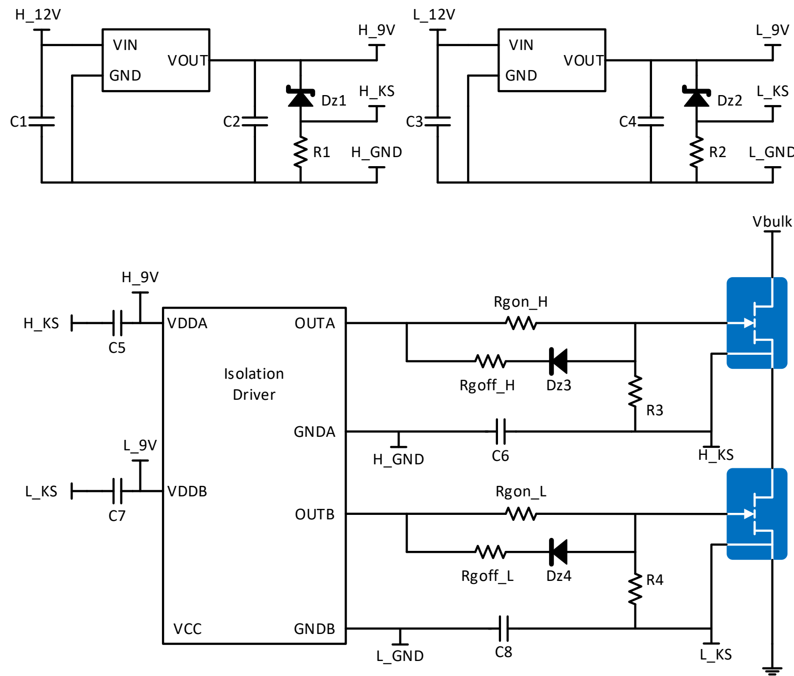


Figure 28 Half-Bridge Driving Circuit with Integrated Digital Isolator and Driver

4.2.2. Functions of Each Components in Half-Bridge Isolated Driving Circuit

Table 11 Functions of Components in Half-Bridge Isolated Driving Circuit

Component	Function
R_{gon_H}/R_{gon_L}	Modify turn-on speed of GaN FET
R_{goff_H}/R_{goff_L}	Modify turn-off speed of GaN FET
R3/R4	Gate pull-down resistor
C5/C7	Turn-On loop Vcc decoupling Capacitor, referred to as Turn-On Capacitor
C6/C8	Turn-Off loop Vcc decoupling Capacitor, referred to as Turn-Off Capacitor

4.2.3. Switching Process of Half-Bridge Isolated Driving

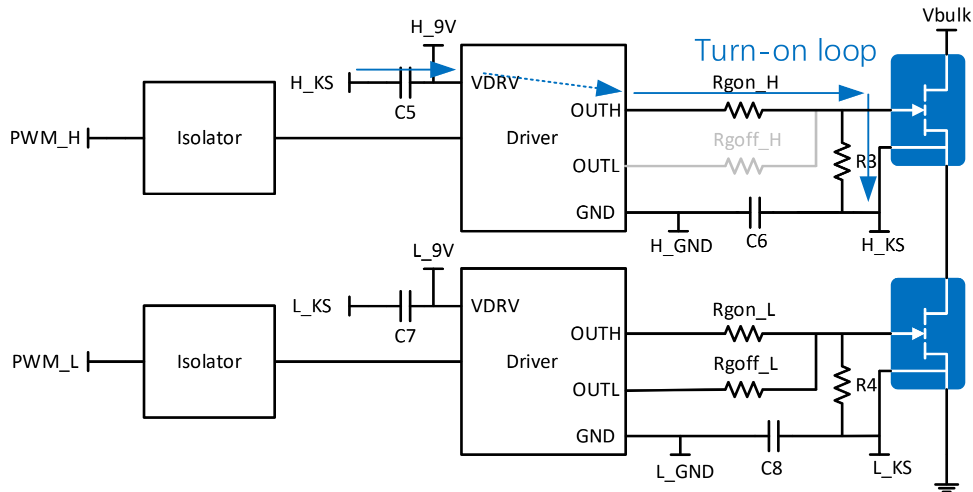


Figure 29 Turn-on loop of Half-Bridge Driving Circuit with Digital Isolator + Driver

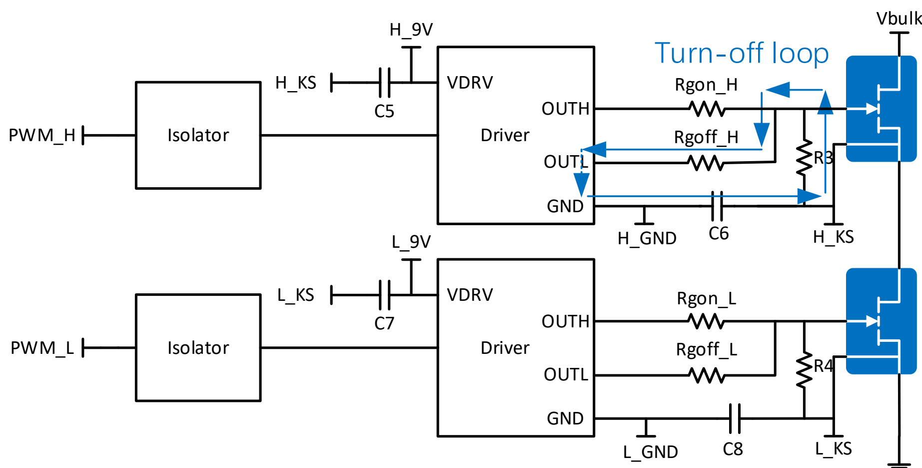


Figure 30 Turn-off loop of Half-Bridge Driving Circuit with Digital Isolator + Driver

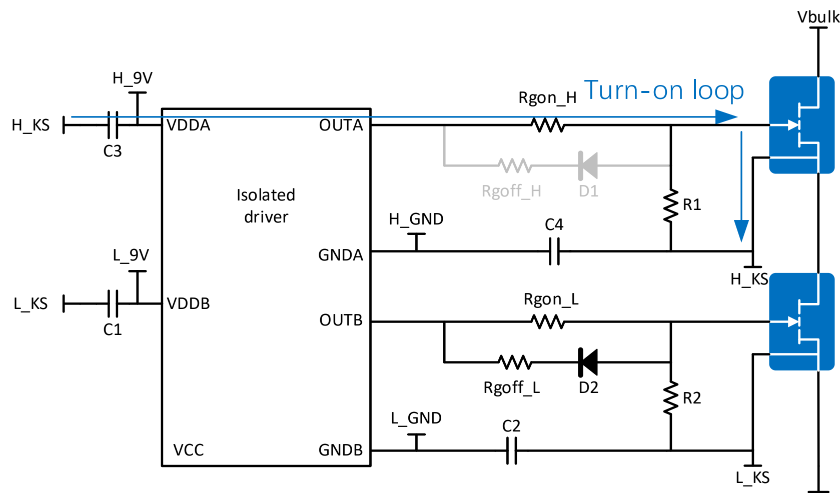


Figure 31 Turn-on loop of Half-Bridge Driving Circuit Integrated with Digital Isolator and Driver

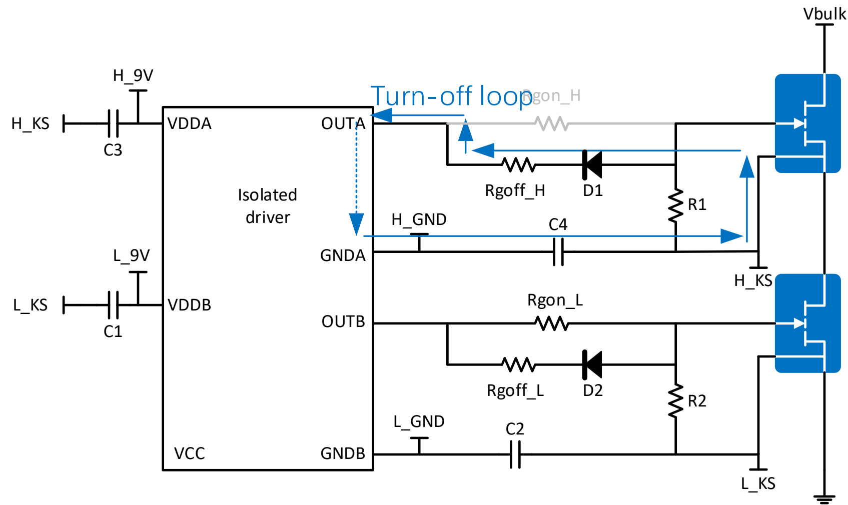


Figure 32 Turn-off loop of Half-Bridge Driving Circuit Integrated with Digital Isolator and Driver

4.2.4. Example of Parameters for Half-Bridge Isolated Driving Circuit

Table 12 Parameters for Half-Bridge Isolated Driving Circuit

Component	Function	Typical	Range
R_{gon_H}/R_{gon_L}	Modify turn-on speed of GaN FET	10R	10R ~ 75R
R_{goff_H}/R_{goff_L}	Modify turn-off speed of GaN FET	2.2R	2.2R ~ 10R
R3/R4	Gate pull-down resistor	10K	7.5K ~ 10K
C5/C7	Turn-On Capacitor	1nF	1nF ~ 3.3nF
C6/C8	Turn-Off Capacitor	2nF	2nF ~ 6.6nF

To mitigate the risk of fault turn-on in the half-bridge driving circuit, it's necessary to use negative gate-source voltage during the GaN FET off-time as shown in Figure 34. The high-level gate-source voltage of high/low-side GaN is determined by the 6.2V zener diodes DZ1/DZ2. The turn-off negative voltage is recommended as -3V which equals to H_VDD/L_VDD - 6.2V,.

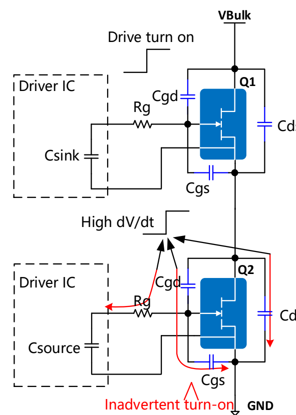


Figure 33 Illustration of fault turn on in Half-Bridge Driving circuit

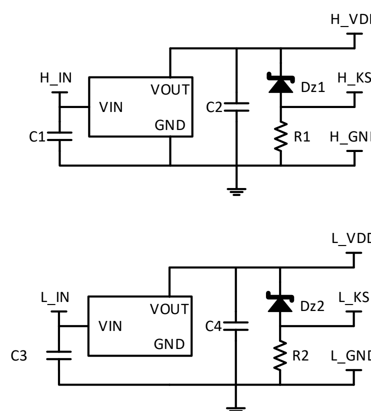


Figure 34 Negative Voltage generating Circuit for Isolated half-bridge Driving

4.2.5. Design Considerations for Half-Bridge Isolated Driver

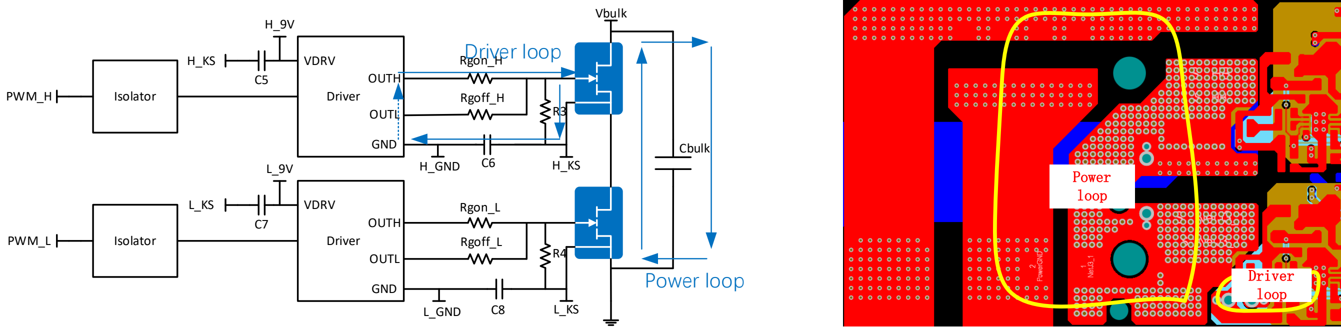
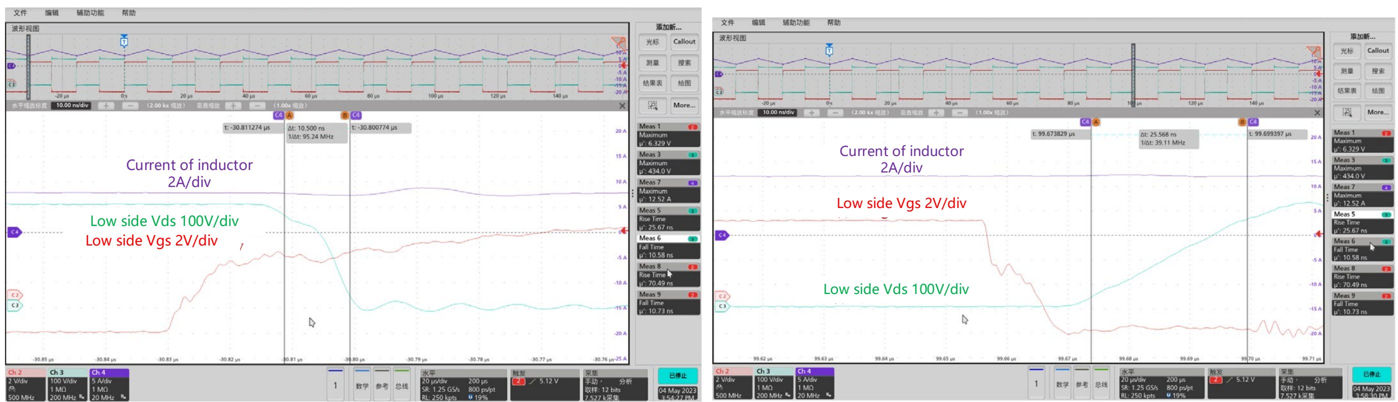


Figure 35 Examples of layout design



(a) Measured turn-on waveforms (b) Measured turn-off waveforms

Figure 36 Waveforms of Turn-On and Turn-Off of Half-Bridge Isolated Driving

- Reduction of The overlapping area between the switching node and the high voltage bus and ground reduces parasitic capacitance on the PCB, effectively lowering GaN switch losses Eoss and Eqoss and increasing system efficiency.

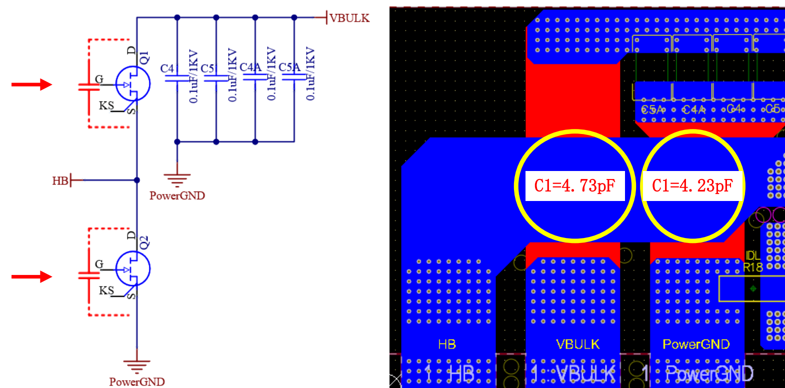


Figure 37 The example of layout with minimized power overlap

- Use Kelvin source design to minimize the coupling between the driving loop and the power loop, and eliminating the influence of

dI/dt from the power loop on the driving loop.

Place the driver IC as close as possible to the GaN to minimize the loop parasitic inductance.

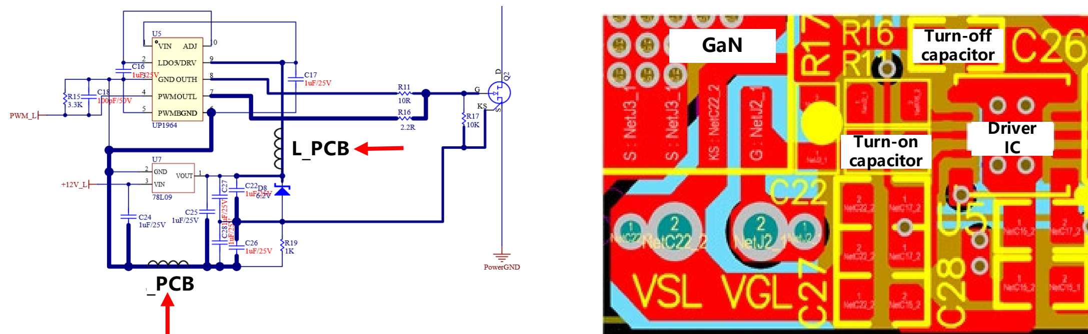


Figure 38 Layout example of decoupling capacitors placed close to the driver

- The driving circuit adopts the overlapping routing method, where the components are placed on the top layer and the first inner layer is used for SK(kelvin source) node to reduce the parasitic impedance in the driving loop.
- The ground impedance coule be significantly reduced by increasing the area of the copper area of SK node thus reducing the impact of parasitic inductance on the driving loop and avoiding the noise coupling between high noise PCB traces and the driving loop.

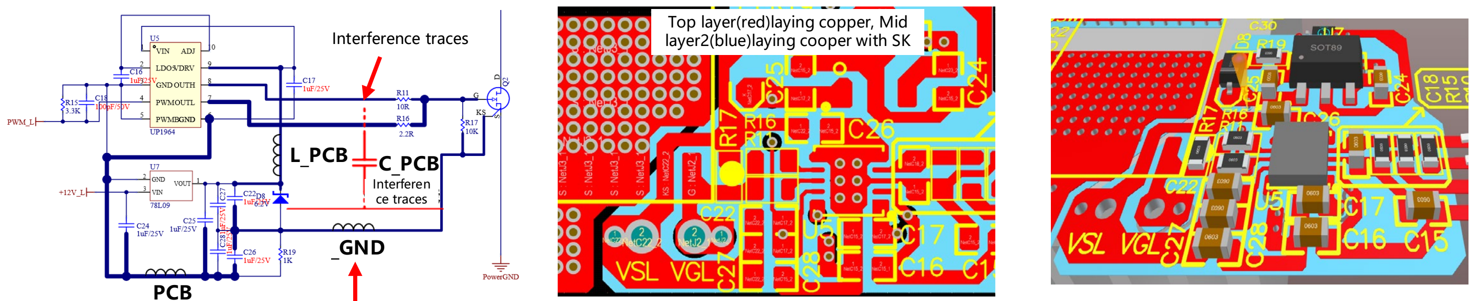


Figure 39 Layout example of overlapping routing for the driving circuit

Appendix

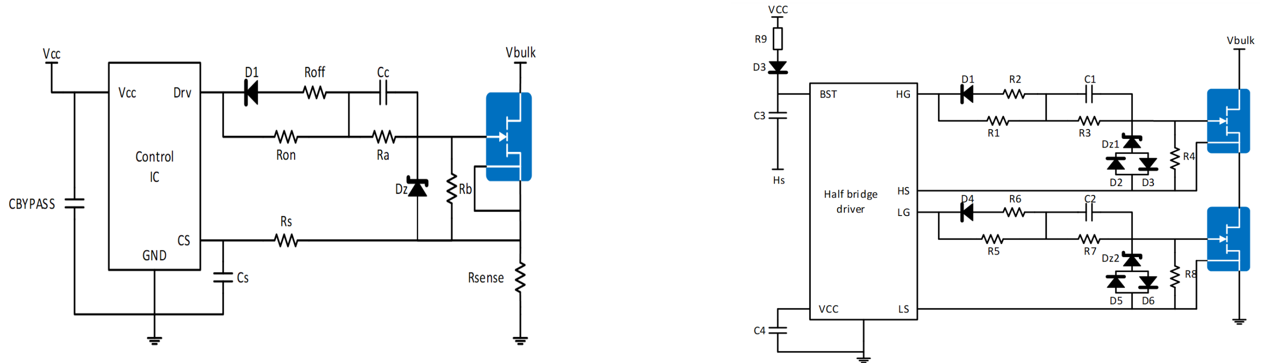


Table 13 Recommended parameters for voltage-divider driving circuit

Component	Recommended typical parameter values						
InnoGaN	INN650DA04 INN650DA480B INN700TH480B INN700TJ480B	INN650D350A/B INN650DA350A/B INN700TH350B INN700TJ350B INN700TK350B	INN650D260A INN650DA260	INN650D240A/B INN650DA240A/B INN700D240B INN700DA240B INN700DC240C INN700TH240B/C INN700TJ240B/C INN700TK240B/C	INN650D190A/B INN650DA190A/B INN700D190B IINN700DA190B INN700DC190C INN700TH190B/C INN700TJ190B/C INN700TK190B/C	INN650D140A/C INN650DA140A/C INN700D140C INN700DA140C INN700DC140C	INN650D150A INN650DA150A
Ron/R1/R5	680Ω	560Ω	390Ω	390Ω	360Ω	200Ω	200Ω
Roff/R2/R6	2Ω	2Ω	2Ω	2Ω	2Ω	2Ω	2Ω
Dz	6.2V, accuracy±2%	6.2V, accuracy±2%	6.2V, accuracy±2%	6.2V, accuracy±2%	6.2V, accuracy±2%	6.2V, accuracy±2%	6.2V, accuracy±2%
Dz1/Dz2	5.6V, accuracy±2%	5.6V, accuracy±2%	5.6V, accuracy±2%	5.6V, accuracy±2%	5.6V, accuracy±2%	5.6V, accuracy±2%	5.6V, accuracy±2%
D2/D3	1N4148	1N4148	1N4148	1N4148	1N4148	1N4148	1N4148
D1/D4	1N4148	1N4148	1N4148	1N4148	1N4148	1N4148	1N4148
Ra/R3	3.6KΩ	3.3KΩ	2.7KΩ	2.7KΩ	2.7KΩ	2.7KΩ	2.7KΩ
Rb/R4	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ	10KΩ
Cc/C1	680pF	820pF	1.5nF	1.5nF	2.2nF	3.3nF	3.3nF

Note: Adjustments may be made to the recommended parameters based on actual conditions to ensure proper driving of GaN in the application system.

Revision History

Date	Version	Description	Check
2024/04/09	1.0	English translation	AE team

Note:
There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.
Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

Reminder:
This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

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